

## REMARKS/ARGUMENTS

The applicants' attorneys appreciate the Examiner's thorough search and remarks.

Responsive to the rejection of claim 9 under 35 U.S.C. §112, second paragraph, claims 1 and 9 have been corrected. Reconsideration is requested.

Claim 1 has been rejected under 35 U.S.C. 102(b) as anticipated by Kinzer et al. (Kinzer), U.S. Patent No. 5,338,693. Reconsideration is requested.

Claim 1 has been amended to call for the following combination:

1. A P-channel MOS gated device which is resistant to single event radiation failure and having improved total dose radiation resistance; said device comprising:

a P-type substrate having substantially flat, parallel upper and lower surfaces;

a plurality of laterally spaced N-type body regions extending from said upper surface into said substrate;

at least one respective P-type source region formed in each of said body regions in said upper surface of said substrate and defining a respective channel region in said upper surface in said N-type body region;

a gate electrode comprised of polysilicon implanted with p-type dopants disposed atop and insulated from said channel region and operable to invert said channel region in response to the application of a suitable gate voltage to said gate electrode said gate being insulated from said channel region by a gate oxide layer comprising silicon dioxide, said gate oxide layer being comprised of radiation hardened silicon dioxide and less than 1000Å thick;

an interlayer oxide disposed over each gate electrode and having tapered profile portions each aligned with a respective P-type source region; and

a source electrode disposed atop said upper surface and connected to said at least one P-type source region;

wherein said gate oxide is capable of resisting threshold voltage shift due to total radiation dose and capable of resisting single event gate rupture due to a single event effect.

Kinzer teaches doping the polysilicon that constitutes the gate electrodes thereof using a POC1 process. As set forth in Kinzer, the deposition required for doping the polysilicon takes place at 925°C. Col. 6, lines 15-19.

On the other hand, in a device according to the present invention, the polysilicon constituting the gate electrodes of the device is doped through implantation. Thus, the gate dielectric is not exposed to a high temperature step, which as is well known, may adversely affect the ability of the same to withstand degradation due to cosmic radiation.

Moreover, claim 1 calls for an interlayer oxide over each gate electrode that includes tapered portions each aligned with a source region. The tapered portions improve step coverage as stated in the specification. Specification, page 11, line 24 - page 12, line 2. Kinzer does not show or suggest such tapered portions.

Kinzer, therefore, does not anticipate claim 1 as it does not show or suggest every limitation therein. Reconsideration is requested.

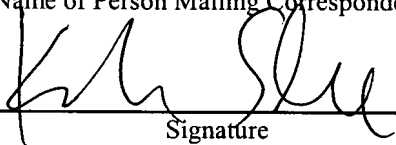
Each of the remaining claims depends from claim 1 and thus includes its limitations as well as other limitations which in combination with those of claim 1 are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

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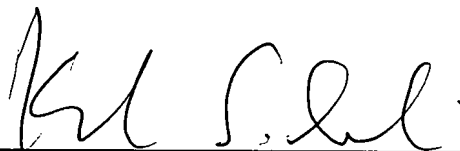
  
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Respectfully submitted,



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